Electronics Status for PDSG

K. Einsweiler, LBNL

Status of 0.25μ work

- DMILL activities and irradiations
- Status of FE-I and MCC-I work, FE-I review
- Next Steps, Schedule, Testing Plans

Opto-chips and opto-links

- DMILL and 0.25μ status
- New 8-in-1 opto-package implications

Power Supplies

- Status and directions for near future

ROD status and multi-module readout support

- ROD prototypes, plans for module interfacing, PLL-based multi-module support.

Rack allocations and USA15/US15

- Present rack request and arguments

DMILL Activities

New FE-D2 wafers from ATMEL

- ATMEL has completed test run with different epi vendors. They will send us 12 wafers with two technology splits, one for epi vendor, one for gate oxide thickness, three wafers of each type. LBL will probe the wafers and send data to ATMEL.

Irradiations of FE-D2S single chips

- Initial results of irradiations showed loss of function after several MRad. Measurements after annealing show that full functionality returns, even for 50MRad irradiation, and digital performance is largely unchanged. However, signs of large changes in analog performance after 100 C anneal step.

Results on MCC-D2

- Event building operates only at about 25-27MHz. Yield is about 10%. No further plans for testing or irradiating.

Results on DORIC-D2 and VDC-D2

- VDC-D2 operated reasonably well under irradiation.
- DORIC-D2 showed several problems. Required very high operating supply voltage (almost 5V), required increase in internal bias, and showed significant increase in input threshold. Some improvements implemented in DORIC-D3 preamplifier to improve front-end performance, but will probably not address all problems.

Comments on FE-D2S assemblies and testbeam

- Wafers were given to bumping vendors in Jan. Only now are assemblies returning.
- Error in sensor bumping mask means that single pre-production sensor chips from IZM will have to wait even longer for bumping of another sensor wafer with the correct mask. Perhaps in August ?
- Should evaluate whether performance of FE-D2S with AMS bumping is adequate for further study. Bumped FE-D1 analog performance was quite poor. First assemblies at Genova seem to behave suprisingly well.
- There are no interesting electronics issues that merit an FE-D2 testbeam effort.
- Effort to use FE-D2S as vehicle for testing irradiated sensors will be considerable, and analog performance of electronics after irradiation is not well-known at this time. Collaboration needs to weigh scale of effort against minor concerns with preproduction sensor.
- Operation of FE-D2S modules will be difficult. Need to determine whether modules can be operated properly with internal threshold control and without TDACs. Only once this has happened does it make any sense to plan for module irradiation.
- Decision of Genova to abandon MCC-D2 means there is no way to build a rad-hard Flex module (perhaps one could use MCC-D0 and operate in transparent mode ?)

Status of 0.25μ Activities

FE-I test chips

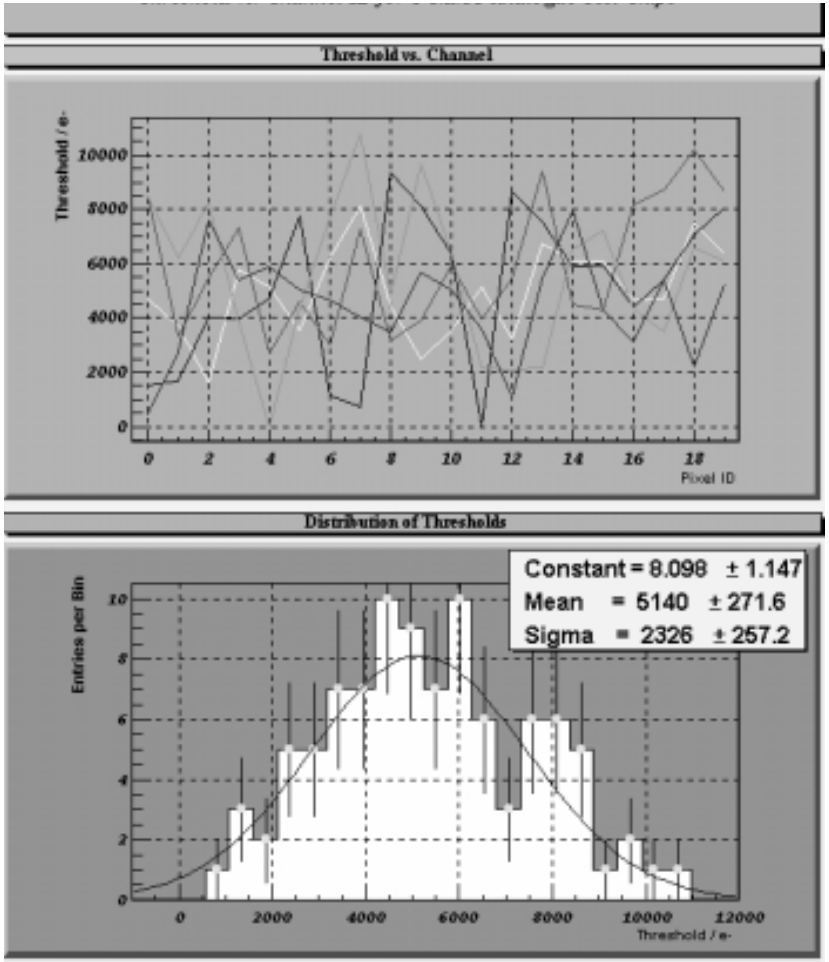
- Major submission of Analog Test Chip Feb 28 to IBM and Mar 5 to TSMC. TSMC chips returned one month ago, and have been extensively tested and irradiated. IBM wafers are presently lost between CERN and the dicer (entered CERN shipping on May 30). If they are truly lost, will take several weeks to get backup wafers from IBM. In any case, will miss opportunity to irradiate at LBL on June 21.

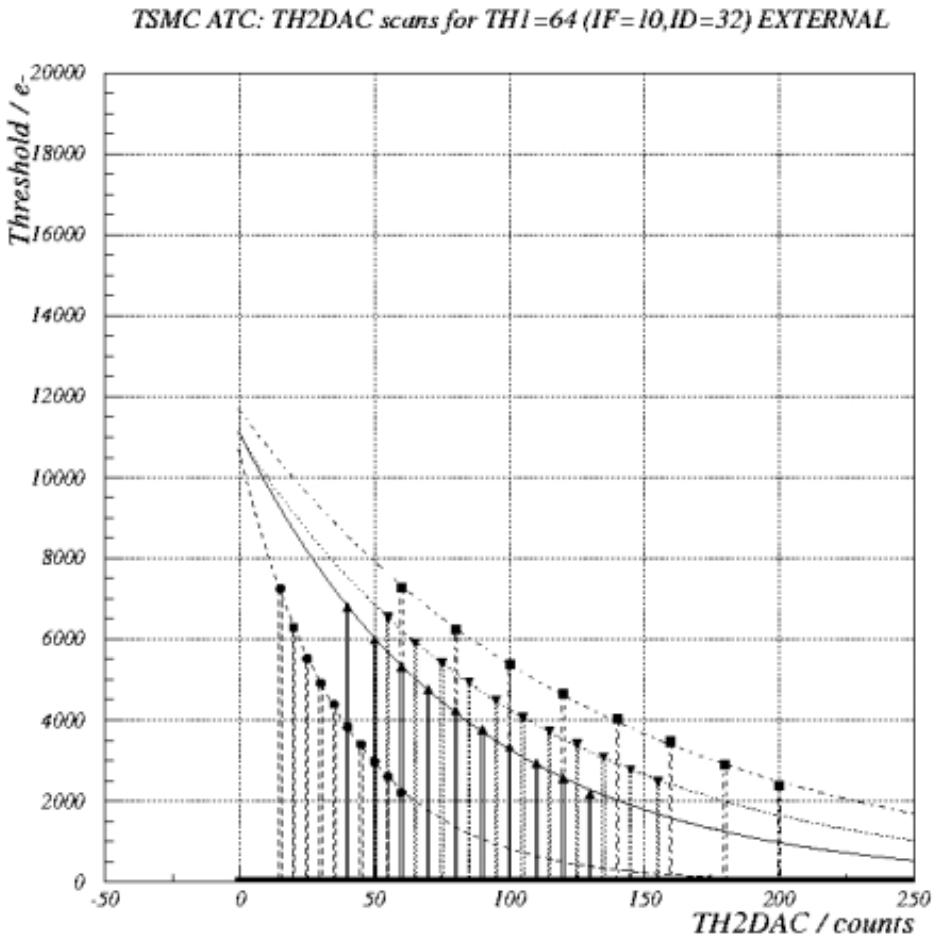
Problems in present test chip measurements:

- Caveat: have tried to extract critical capacitance values to determine scale, but the values used have some level of uncertainty.
- Threshold dispersion is unacceptably high. Only have 20 pixels per chip, so took average over 5 chips, and found RMS of 2300e. This is five times more than desired, and at least twice the maximum acceptable level.
- Noise values are high, leading to estimates of 400e with 400fF sensor, and 500e with 50nA on 400fF sensor. Specification is 300e for this.
- Minor issues in charge injection circuit (possibly related to sensitive strobe generation on test chip) and LVDS driver (needs further study).
- Need to verify measurements in more detail, and to compare to IBM test chip results (no differences expected).

Does front-end meet specifications ?

- Except for threshold dispersion and noise, answer appears to be yes. Noise is marginal, threshold dispersion is unacceptable. Timewalk, leakage compensation, TOT performance all appear to be very good (same for other analog/digital blocks).
- Measurements of threshold dispersion in five test chips (left) and measurement of variation of threshold with threshold control for 4 pixels:

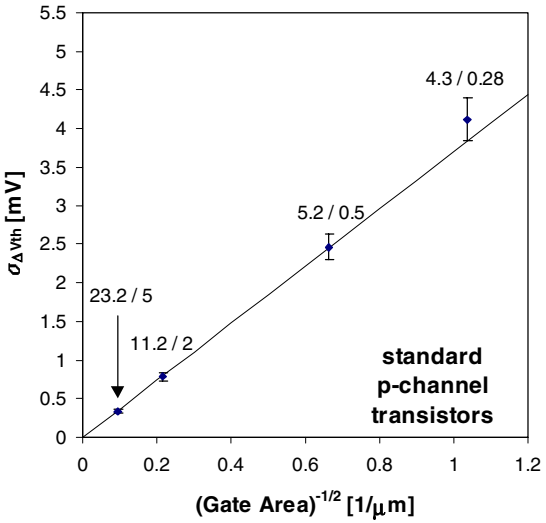


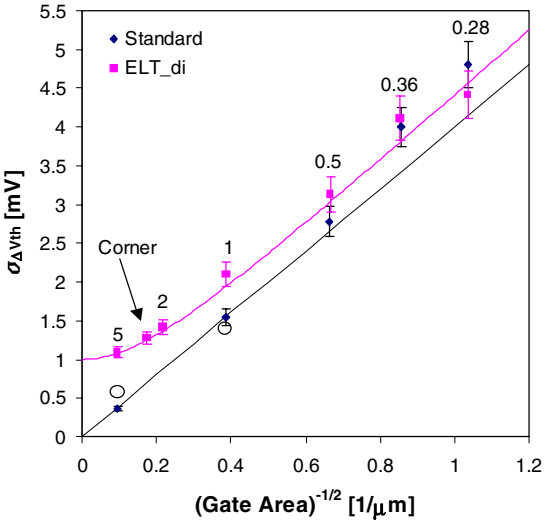


Threshold dispersion and matching:

- Have carried out first studies of impact of VT matching on present front-end, as a possible explanation of the large threshold dispersion.
- First simulations just used a voltage source to shift the VT of each critical transistor in the preamplifier and second stage by a known amount, and then scaled to the expected VT mis-match for that device. There are 10 sensitive FETs in the preamplifier and 4 in the second amplifier. This gave a crude estimate of 1500e threshold dispersion, by looking at DC baseline shifts at the discriminator input.
- A more sophisticated analysis has been done by Peter Denes by actually injecting charge and scanning to find the discriminator threshold for each simulation. This gives a set of curves which show similar features to those seen in the data.
- A more extended Monte Carlo run was then performed, where each device had its VT modified using a Gaussian with sigma taken from the thesis of G. Anelli:

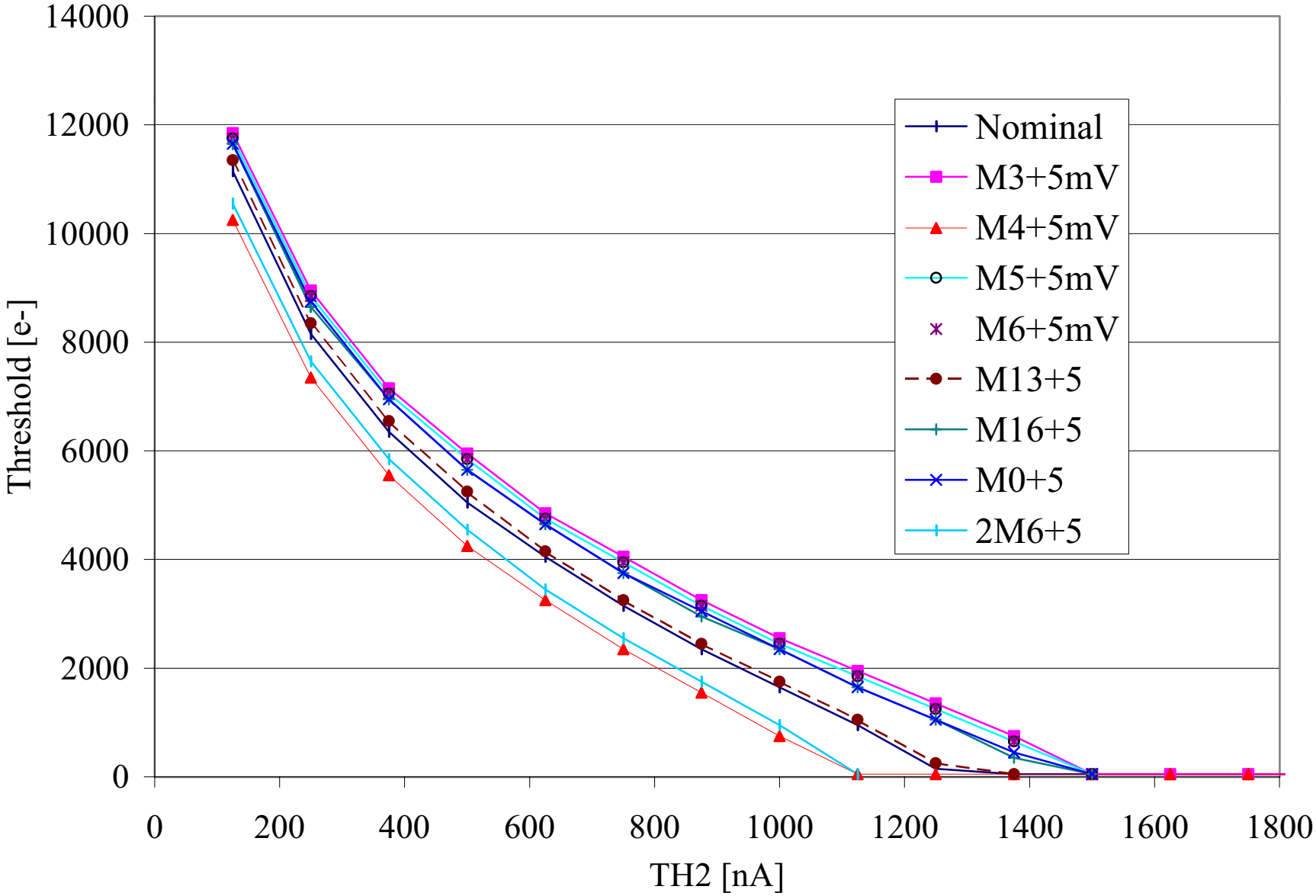
Standard PMOS VT matching versus device size





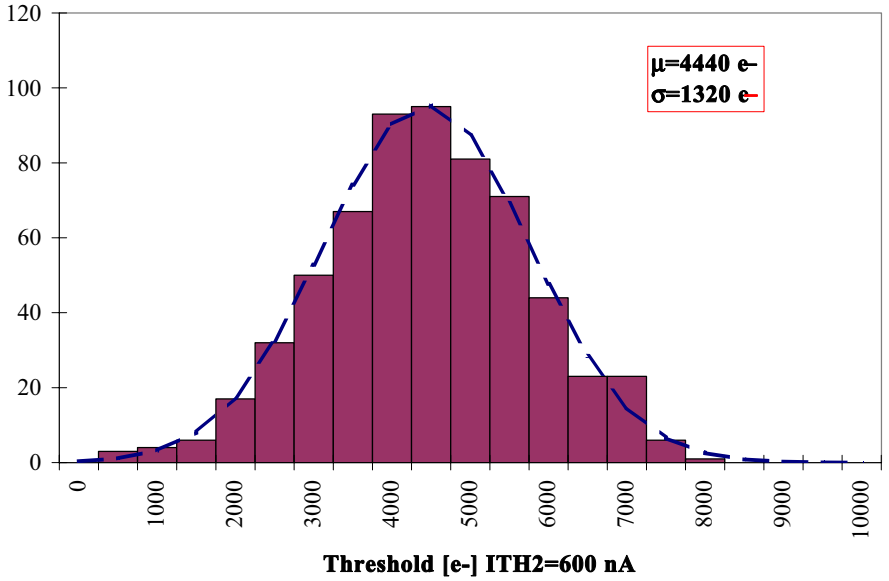
Enclosed NMOS VT matching versus device size

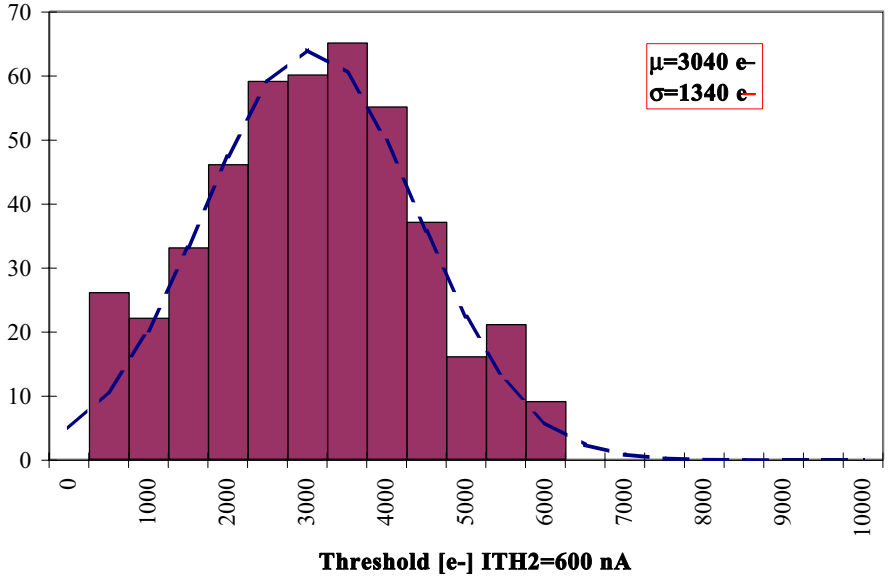
- Threshold simulation, moving each device by ΔVT = +5mV:

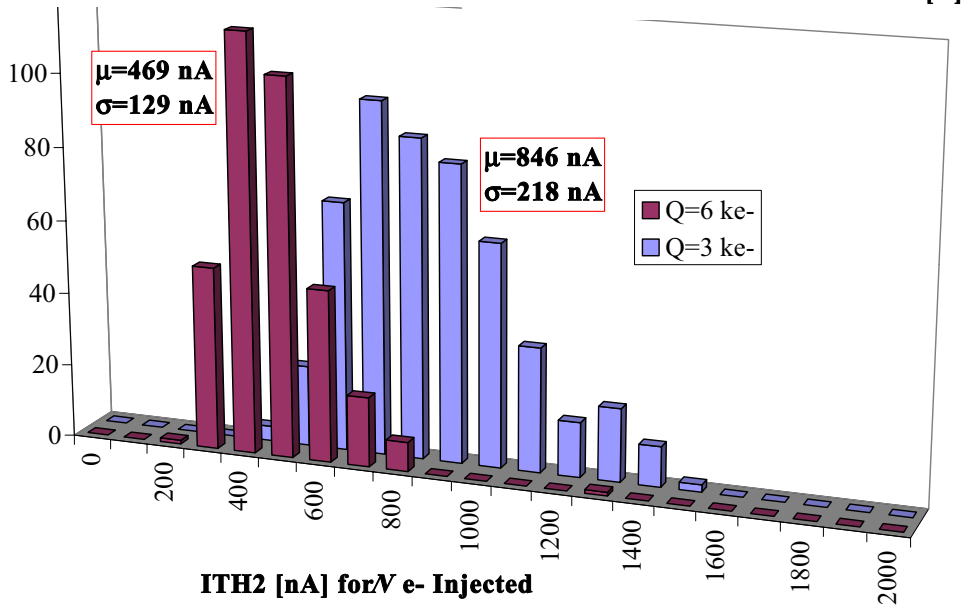


- Need to combine contributions in quadrature, but behavior looks like measurement.

- Results of Monte Carlo simulations for different ITH2 and different Q(inj):







- Have not included sources of chip-chip variations, but matching contributions can clearly explain a large fraction of the excessive threshold dispersion observed.

Reticle for FE-I Run

Similar to FE-D2 run, all designs should use same pads

- **Two FE-I chips:** the present plan is that these would be identical.
- **MCC-I chip:** this should be the complete new MCC with U-pinout to satisfy module constraints. For the purpose of making a reticle, it would be simpler to dice if the long dimension was no more than the width of an FE chip (7.2mm)...
- **DORIC-I and VDC-I chips:** they would be improved versions of the designs submitted in the Feb MPW run.
- **Analog Test Chip:** this should be very similar to the test chip just fabricated, but would contain the final design and layout of all analog blocks, and perhaps 64 channels instead of 20. We should attempt to keep a similar pinout.
- **LVDS Buffer Chip:** this is a convenient way to include the interface between a single chip and our test system into a rad-hard chip. Given the absence of commercial LVDS drivers operating at less than 3.3V, this is even more useful. It contains 4 LVDS->CMOS converters, 3 LVDS->LVDS converters (3.5mA outputs) and possibly a buffer for the MonAmp pin (depending on how this is handled in the FE-I chip).
- **PM bar:** may be useful for checking details of device characteristics, although the very good parameter stability seen so far suggests it may no longer be needed. It is more likely that we will just include the small bar designed by the CERN group, and used by them to track the parameter stability on all multi-project runs.

Common Engineering Run

Processing options defined:

- Five metal layers, with LM top metal (1.0μ, 30mΩ/sq) and TV passivation (1.0μ, oxide/nitride).
- No backside grinding, so wafers will be left at their native thickness of about 700μ.
- Additional masks for special features: OP Resistor (silicide block for poly resistors, ESD output drivers), MiM Capacitor (high value linear capacitor made with additional Q2 layer).
- Request 12 wafers (nominal maximum for an engineering run is 6) under informal agreement with IBM. This will provide us with enough wafers for multiple bumping vendors, MCC commercial IC tester screening, etc. Second set of six wafers would be delivered several weeks after the first.
- Possibility of “striping” is interesting. Vendor uses standard processing in central 80% of wafer, and does +/-1.5 and +/-3 sigma variations of a single parameter on the rest. This option needs further discussion to understand possibilities.
- Approximate total cost 190K$. Exact amount will be known soon from IBM quote. Purchase Order will be issued by CERN from their standard foundry account, and TID’s will be used to collect money from specific institutional accounts in ATLAS pixels. This allows all preparation to proceed without signatures.

Present Status

ATLAS review of FE-I

- Review took place at CERN June 6-7. Reviewers were Anghinolfi, Campbell, and French (Campbell dropped out due to prior committments).
- It is clear that this review, scheduled back in Feb/Mar, was too early for us. However, we decided to go ahead, and we will have a brief follow-up review prior to submission.
- Presented designs and all measurements to date, plus plan for finishing the chip. This was very useful, and pretty well filled the two days. We learned a number of things.
- We need very much to write a complete specification for the FE-I, against which its performance can be judged.
- Our major concern at the moment is to understand the very large threshold dispersion observed in the TSMC Analog Test Chip. We hope to receive the IBM version of the chip in the next few weeks.
- We should receive a written report from the reviewers shortly.

ATLAS review of other chips (MCC and DORIC/VDC):

- Review of these chips is necessary, and should naturally have been scheduled along with the FE-I review. Propose to conduct FDR on all designs after results from first 0.25μ run become available, in roughly early 2002.

Status of FE-I Integration

- Layout/integration of front-end blocks and analog bottom-of-column almost complete. This includes 12 DACs, bias mirrors, and current reference. Integration of buffering and logic for the control section started but not yet complete. The test pixel support (MUX and buffer) not yet integrated, but blocks exist in the test chip.
- Now plan to also integrate significant decoupling (several pF per pixel on both analog and digital supplies) into each column pair, and will likely modify the present shielding scheme somewhat.
- Layout of digital readout is complete, including CEU, sense amplifiers, and TOT processor. Have performed TimeMill simulation of this circuitry for a complete column pair with full parasitic extraction, and the performance looks good.
- Layout of EOC buffers (presently 40 per column pair) and MUX sparse scan of column pairs is complete. Could add more buffers for a total of 64 if needed.
- Power budget for digital supply looks OK (10mA for column readout, 7mA for EOC buffers when idle). PowerMill being used to study dynamic consumption.
- Performing final updates on Verilog descriptions of blocks at the bottom of the chip (Readout Controller, Clock Generator, Command Decoder, Global Register, Grey Generator, Reset Generator, Output MUXes). These blocks will then be synthesized and placed and routed.
- Additional special blocks (smart decoupling, overvoltage protection, regulators, and capacitor measurement) are in progress at Bonn.

Status of MCC

- Verilog aspects of design have been completed and validated with SimPix.
- Custom blocks (FIFO and Delay) complete or almost complete.
- Test vector generation and simulation is ongoing, but not complete.
- First pass at overall layout has been made, but it needs refining.
- Still need to back-annotate parasitics and check performance.
- Final step is all of the technical verification (LVS, DRC).
- Giovanni estimates one month of work left. This seems optimistic, but should be less than two months (back-annotation on this scale is challenging).

Status of DORIC-I and VDC-I

- Submitted first version (DORIC-I1, DORIC-I2) in Feb IBM MPW. Die not back yet.
- The design is basically the same as for DORIC-D2 and VDC-D2, but with minor improvements in DORIC (better preamp feedback to eliminate offset problems) and VDC (bright/dim current generation).
- Need to evaluate test chips and implement any necessary changes. There are also new optimizations of preamp design. Should implement pixel pads for improved ESD protection and lower-voltage LVDS I/O.
- Need to consider optimization of die size, and possibly multi-channel chips, to match new opto-package baseline of Taiwan 8-in-1 (1mm pitch for opto-elements).

Estimated submission date:

Issues raised so far by the test chips:

- Large threshold dispersion observed. Calibration scale not yet definitive, but range of dispersion is sigma of 2000-2500e. Studies suggest matching of small current mirrors is a major factor - there may be others. Not clear how much improvement will be possible with modest modifications in the design - perhaps a factor two.
- Need for new chips limits the time available to improve the present front-end design to a maximum of about 2 months. This timescale prohibits major design modifications, and only allows optimizations about the present design.

Remaining tasks:

- Continue characterization of test chips to learn as much as possible about the present designs, including irradiations.
- Improve transistor matching in front-end to maximum extent possible. Understand and address issues with new chopper design and new LVDS design.
- Finish the overall layout by integrating all present blocks together. Estimate this will take about 4 more weeks. Additional work on front-end almost certainly needed.
- Top level simulations using Verilog for functional verification and TimeMill for timing verification have started, but estimate another 4-6 weeks of work here.
- Formal verification (LVS and DRC) will also take several weeks. Estimate that with significant effort, could submit roughly 2 months from today.

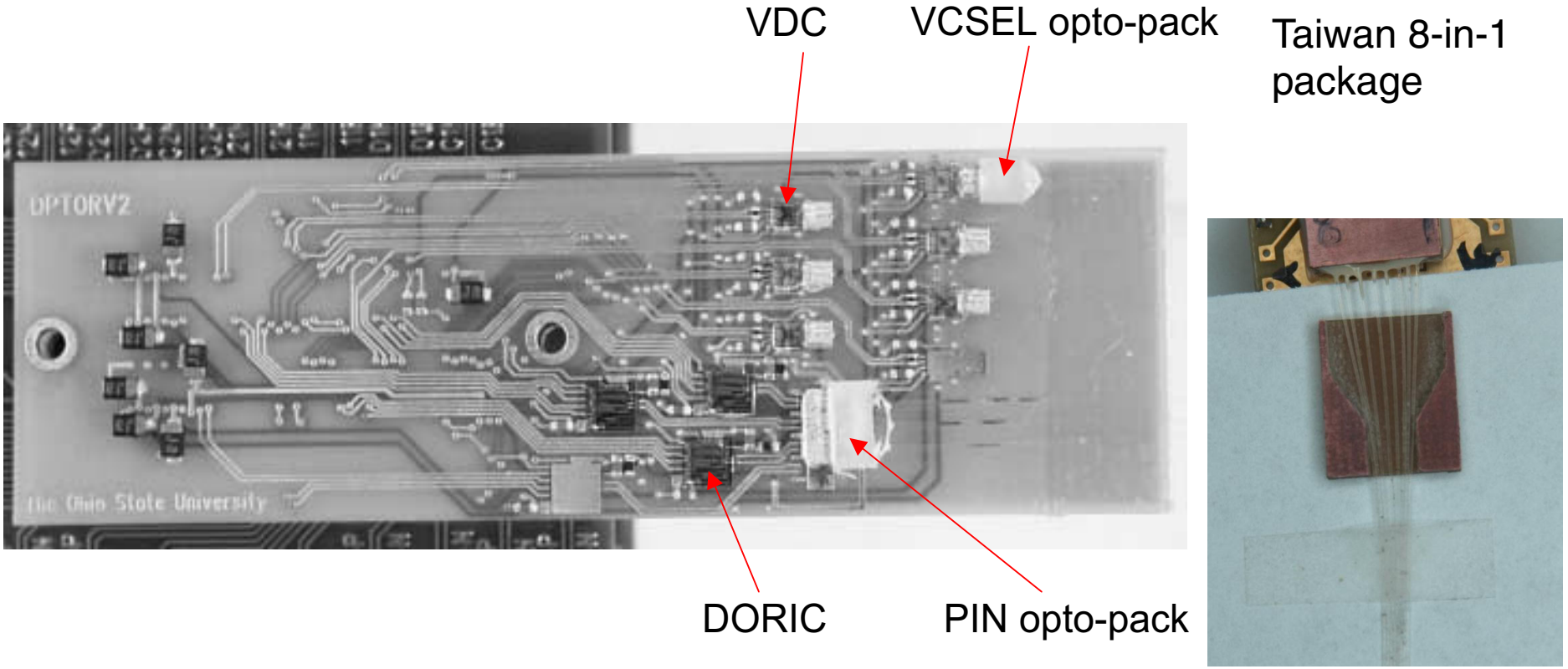
Opto-chips and Opto-links

Opto-chips:

- Opto-electronics is presently pursuing two paths, DMILL and 0.25µ.
- For DMILL path, opto-electronics group has recently participated in MPW run and submitted DORIC-D3. This includes improvements in preamp to eliminate problems with DC offset that presently produce “good” and “bad” DORICs.
- Major concern with 0.25µ path is whether the maximum 2.5V power supply for the chips will be adequate to bias irradiated VCSEL with 20mA. For Mitel VCSEL, information suggests it is marginal. Information not available yet for Truelight VCSEL.
- The opto-electronics effort needs to be reviewed. This could be an FDR and a technology choice together, and would propose to aim for early 2002 date.

Opto-links:

- With Taiwan 8-in-1 package choice, need to move towards final configuration for opto-chips and opto-card. Present card from OSU for their package:



- New package is roughly 10mm wide and 8mm deep. Taking advantage of this package for the PINs requires modifying the present DORIC layout.
- Either use rectangular single-channel layout (long and narrow), or consider implementing a multi-channel version (mixed-mode issues would be important).
- B-layer requires two data links on one side, one control link on the other.

Power Supplies

Status of vendor prototypes:

- Complete CAEN A1509 unit delivered last year, and recently characterized by pool. Minor problems found, but basic performance looks acceptable. New proposal from CAEN for CMS Tracker, based on more distributed approach to reduce cost (standard mainframes are expensive and not needed for large systems).
- Prototype ISEG HV supply (8 channels) has arrived, and is in the pool for testing. Some control problems appeared that need to be resolved with vendor.
- DPS prototype module available within the next month for evaluation.
- Wiener has new LV system under development, which looks interesting for ATLAS. Will follow developments. This would be used in combination with ISEG.

Prototype results:

- Important study in Milano of operation of CAEN A1509 unit with current sensing. Measurements make it clear that this type of sensing is not really feasible with multiplicity two. Incorrect regulation and transient behavior observed when one module is switched off. This behavior seems fundamental to this scheme.
- First look at remove voltage sensing with full cable length and CAEN unit indicates that it could work, and should be investigated further. Also this sensing scheme requires modifications for multiplicity of two operation, but information is available to try to do this properly (average two remote sense inputs when both enabled ?)

Many system designs under discussion:

- Supplies in USA15 with current sensing (line drop correction based on resistance), with a multiplicity of two pixel modules per complex channel in the power supply. Maintain services modularity of one back to USA15 to leave open future upgrades.
- As above but using remote voltage sensing (requires two extra lines per supply returning to USA15).
- As above, but with the addition of regulators at PP2, operated in remote sensing mode. Regulators are multiplicity of one per pixel module. No sensing would be done between USA15 and PP2, but services would remain multiplicity of one.
- Use DC-DC converters close to the detector and bulk supplies in USA15. Converters isolate completely at PP2, allowing connection of grounds afterwards with no major implications for star topology of detector grounding scheme.
- Use serial powering scheme with current supplies instead of voltage supplies. This scheme has no grounding (all modules must float), and no means of controlling or monitoring voltage/current at individual module level. All connections (HV bias and optolink data/control) must also be floating.

Much discussion on these issues...

Proposal for how to proceed with Power Supplies:

- Reference design (baseline is too strong a word) should be to have complex channels in USA15 and regulators at PP2. For services, the sensing from the pigtail to PP2 would be adapted to requirements of ST regulator (large sense return needed for regulator power). Small sense pairs would continue to PP3 for connection to DCS for monitoring purposes.
- Multiplicity two approach suggests current sensing is not viable, so drop further work on this for now.

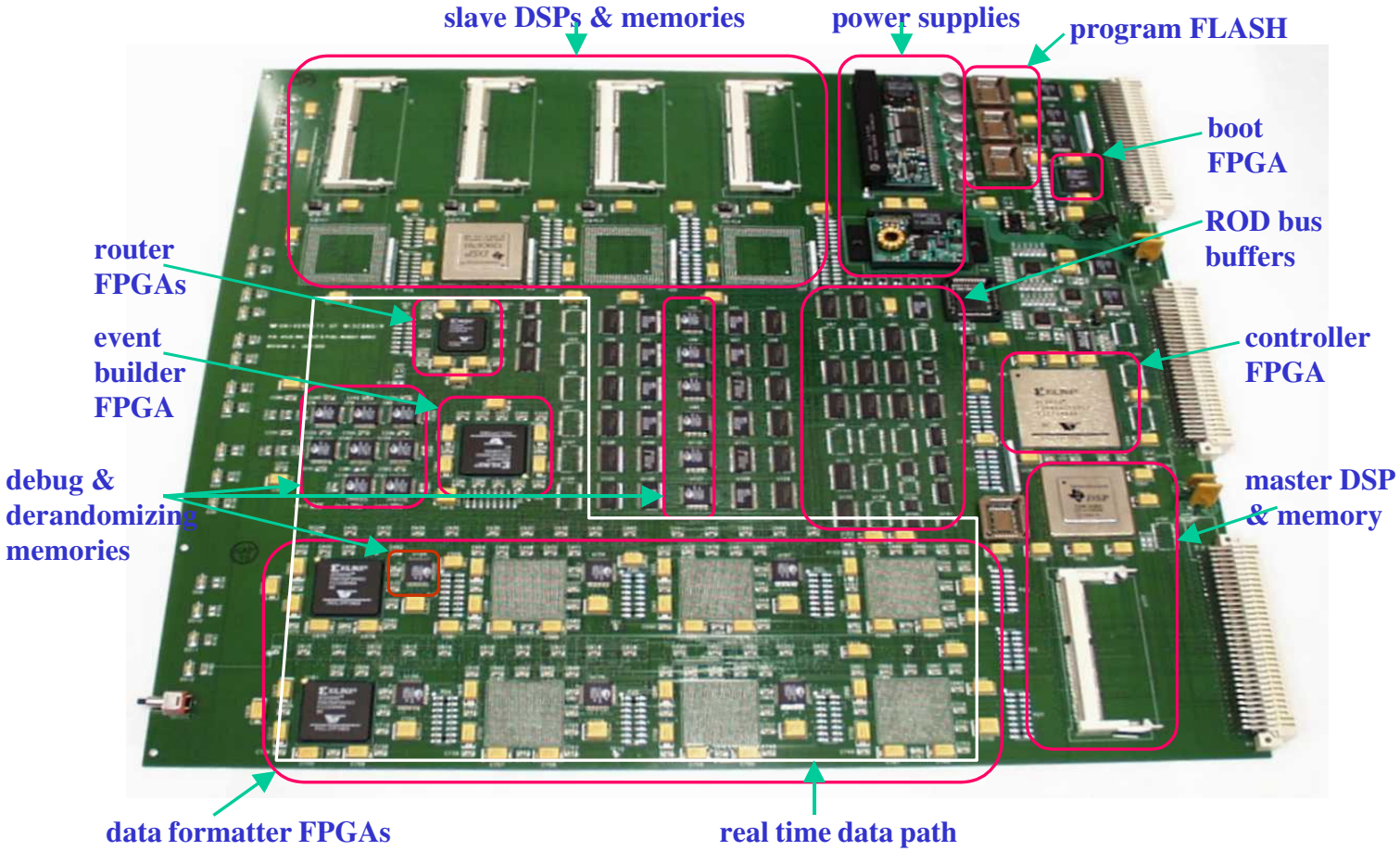
Next steps:

- Continue to work on regulator design. Present situation with ST delivery is very poor. Fourth generation prototype also had problems, now fabricating fifth generation. Samples expected in early Fall, fully qualified parts expected in late 2001/early 2002.
- Investigate other implementations of regulator scheme. In particular, “hybrid” approaches with separate controller and pass element. Examples include use of National regulator core plus Intersil rad-hard PMOS pass transistor, as well as specialized vendor solutions.
- Begin detailed design and layout of PP2 including integrated regulators. Address relevant cooling and connector issues.
- Carry out further studies of remote sensing over full cable length to see whether this is a viable option in case problems with the regulator scheme are not solved.

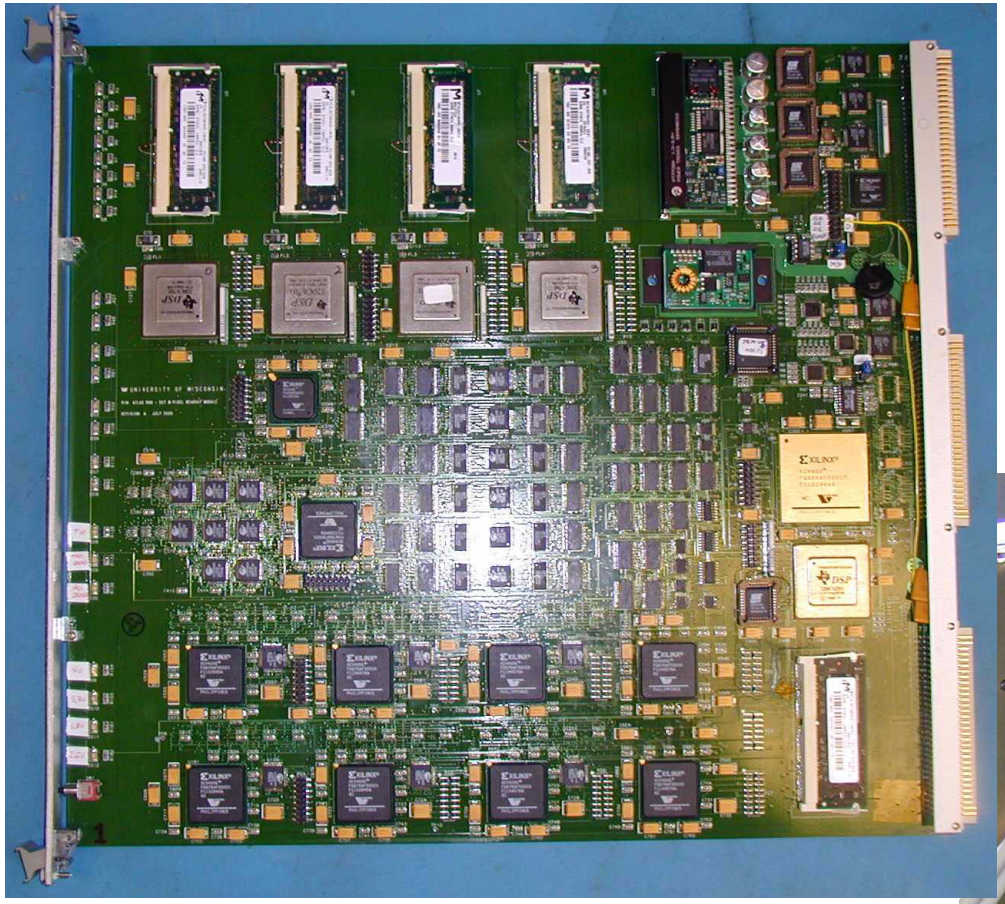
ROD Status and Multi-module Readout

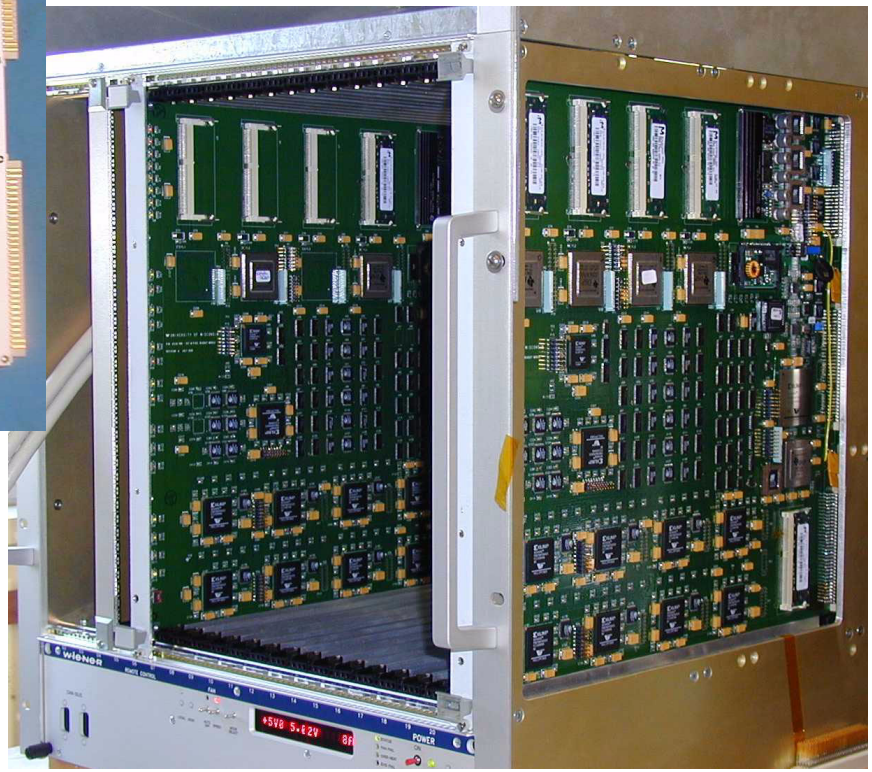
Extended report on ROD status available in EDMS. Summary:

- ROD prototypes are almost completely functional. System level integration of ROD, TIM, BOC, ROD Crate, and RCC processor will begin next week in Cambridge.
- Accumulated changes will be implemented in a new board revision. Expect that these boards will become available to the pixel community in the Fall.



Fully loaded ROD and ROD Crate with two RODS:





Pixel ROD Evaluation:

- Will start from LabWindows test environment created by Lukas at LBL, and add some of the PixelDAQ functionality. This should allow us to operate a ROD in a lab-test environment, with some of the PLL capabilities that we are used to, for example doing threshold/timewalk/TOT scans of modules.
- We would plan to perform initial evaluations of the ROD in the lab using existing modules and a “PCC-like” connection to the BOC connector. This allows use of present support cards containing single chips and modules. Eventually, the goal would be to use the 3-module disk sector that we are constructing from Flex2/FE-B modules as the device to test.
- The next step should involve a more complete system test, including realistic pigtails, a PP0 cable with an opto-daughter card with 6/7 optical links, and a real service bundle for a half-stave and/or a sector. Ideally, this type of “system test” should be prepared in two places (one for barrel and one for disk). Clearly this will not happen until the era of FE-I modules. However, it is time to begin planning and preparing, as there are many different components involved.
- Should imagine trying to use ROD in testbeam in 2002. This will require some planning and preparation.
- Hope that DAQ development can proceed in the direction of a common SCT/Pixel DAQ framework based on ROD and DAQ-1. This will be discussed at the ROD Software Workshop next week in LBL.

Multi-module Testing

Simple solution:

- Propose that for a simple solution, scalable up to a half-stave or a sector, could develop multiplexing PCC configuration for new generation PLL system.
- Provide, for example, 7 output 50-pin connectors with multiplexing support. Control would involve analog MUX for NTC connections, individual enables for XCK, and separately for other output signals, and digital MUX for return signals.
- This would allow PixelDAQ to configure up to 7 modules sequentially. Only one module could have its return data stream connected to PixelDAQ for analysis. Any combination of the seven modules could have XCK only, or XCK plus control signals (LVL1, STR, SYNC) distributed to it. This creates simultaneous activity.
- All 7 module power supply inputs would be separate. The 50-pin connector with 30 AWG flat cable is not ideal for powering modules (voltage drops). Could provide 30-pin ELCO interface similar to PP0, allowing connection to Type 0 cables.
- Major software issue would be PixelDAQ support for configuration data. Need to develop more standard description that could serve PLL and ROD.

High performance solution:

- Use ROD and complete ROD crate.
- Initially, use PCC-like Back-of-Crate card and copper connections.
- Implement PP0-like optical interface in the not-so-distant future...

Rack Allocations and Locations

Requested rack allocation in USA15:

- ROD racks: 4 required for 120 RODs, plus 1 required for ROD test stand.
- LV/HV supplies: 10 required using current estimate of complex channel density. Requested total of 18. Twelve for LV/HV, four for expansion in case of modularity one, 2 for additional control and support functions.
- UPS/DCS: requested 2 racks for DCS and 2 racks for specialized UPS.
- Total request was for 27 racks.
- We were granted 4 racks in ROD area and 15 racks for LV/HV/DCS.

What next ?

- Possibility to have additional space in US15, on the other side of the ring.
- Have requested additional 8 racks there, to reach our initial request of 27 total.
- Need to decide soon whether we are serious about using US15 or not.

Personal judgement:

- Believe that we have (marginally) adequate space in USA15.
- Disadvantages outweigh the advantages of US15.
- We should concentrate on fitting in USA15...

Why Go To US15 ?

Cable lengths:

- Present estimates are based on estimates from Eric Anderssen last year.
- Maximum cable length decreases from 140m to about 120m. This is because cables on US15 side of ATLAS do not need to cross over the detector.
- Average cable length change more difficult to estimate without detailed routing information. Eric's estimate was 10-15m reduction in average length.
- For long Type 4 cables, this is a 10-15% cost reduction (few hundred KCHF ?), and a reduction in the worst run of 15% (mainly risk in operation of supplies).

Rack allocations:

- Space in USA15 is quite precious. We did not receive our full request (5+18+4), but only (4+15), so we are missing 8 racks from what we would like. According to the ATLAS database, there is only one unallocated rack in USA15.
- If we squeezed down to our present best estimates, with no contingency, we could probably fit in USA15. Would have 4 ROD racks, 10 PS racks, 1 controller rack, and 4 DCS/UPS racks.
- For now, have reserved 8 racks in US15 to reach our initial total of 27 racks. Assume that no ROD, DCS, or UPS functions would move. Only LV/HV power supplies would be placed in US15.

Disadvantages of US15:

- May have to wait 1-2 days for access to fix broken equipment.
- Can never be present during beam operation for debugging purposes.
- Interlocking system will require some cable plant between the two locations: